
ECE-C574 ASIC Design I
Winter
Prof. Baris Taskin

Syllabus
Lecture: 1h50m
Lab: 1h50m

— Course Information

Course Title: ASIC Design I
Course Type: Graduate
Credits: 3 credits
Duration: Winter Quarter
Succession: ECE-C575 ASIC Design II

— Instructor and TA Information

Instructor: Prof. Baris Taskin
Office: Bossone 413F
Office Hours: By appointment, taskin@coe.drexel.edu
Teaching Assistant: Ying Teng, Bossone 324

— Audience

This is an MS-level graduate course. This course is cross-listed with ECE-C474, which is intended for senior-level ECE undergraduate students. Workload for graduate and undergraduate students will be different and two parties will be evaluated independently.

— Prerequisites

This course has no prerequisites. ECE-C571 Introduction to VLSI Design is not a prerequisite.

— Course Description

This is a course in the field of *Very Large Scale Integration (VLSI) circuit and systems design*. Design and analysis of VLSI integrated circuits will be covered from a system design perspective. This course will focus exclusively on digital CMOS Application Specific Integrated Circuit (ASIC) systems design and automation. The ASIC physical design flow, including logic synthesis, floorplanning, placement, clock tree synthesis and routing will be presented. These back-end physical design flow steps will also be covered through hands-on practice using industrial VLSI CAD tools.

Course topics include:

1. Implementation Strategies for Digital ICs
2. Logic Synthesis
3. Floorplanning and P/G routing
4. Placement
5. Clock tree synthesis
6. Routing
7. Multi-corner/multi-mode analysis

8. IC Interconnects

9. Multi-voltage design

Note: Topics 7 and 9 are only for ECE-C574 students (i.e. not for students enrolled in the cross-listed undergraduate course ECE-C474).

Teaching Outcomes

Course objectives (i.e. teaching outcomes) include:

- To learn the advanced concepts of modern VLSI circuit and system design, including differences between ASICs and FPGAs, standard cells, cell libraries, IPs etc.
- To have experience with a logic synthesis tool for mapping RTL onto a cell library,
- To understand the back-end physical design flow, including floorplanning, placement, CTS and routing,
- To get accustomed to VLSI CAD tools and their usability,
- To understand the role of computer-aided design (CAD) tools in automating the design flow and providing improved productivity in VLSI systems design.

Course Structure

Recitations: *None*

Laboratory: Once a week, multiple lab assignments

Exam(s): One (1) midterm and one (1) final examination

Project(s): *None*

This is graduate level class and the evaluation criteria is established accordingly. The evaluation process will encompass the monitoring of not only the quality of individual work but also participation in group projects and lectures. The final grade will be calculated as follows:

Final	→	30%
Midterm	→	25%
Lab assignment(s)	→	40%
Participation	→	5%
<i>Total</i>		<i>100%</i>

Note that this course is cross-listed as a graduate level course. Graduate and undergraduate course work will be *different* and students will be evaluated *independently*. Graduate students will have more or different questions on the homeworks and examinations.

The instructor and the TA will provide feedback on any assignment submitted on time within a week. For late submissions, with or without additional penalty issues in grading, the feedback will be provided within the next month. For lab work that was started (and worked on) during lab hours, immediate feedback will be provided by the lab instructor (TA and/or instructor). There will be minimal to no feedback during the lab hours on lab assignments that belong to previous weeks. The in-lab feedback typically consists of corrections to student work and personal instruction. The feedback outside the lab meeting hours are typically a repeat of the instructions given during lab time for the assigned lab work and resolving potential system errors, but not correction of errors in student work.

The Academic Policies of Drexel University Office of the Provost dictates the scale of letter grades <http://www.drexel.edu/provost/policies/grades.asp>. Below are the percentages to be used in assignment of these grades:

Letter	Grade percentage
A+	100 – 97
A	96.9 – 93
A-	92.9 – 90
B+	89.9 – 87
B	86.9 – 83
B-	82.9 – 80
C+	79.9 – 77
C	76.9 – 73
C-	72.9 – 70
D+	69.9 – 67
D	66.9 – 63
F	Below 63

The instructor reserves the right to adjust the grade percentages (e.g. based on the distribution of grades) to accomodate non-standard (low or high) distributions.

Textbook

Following is a list of suggested textbooks for this course, starting with the *required* textbook by J. M. Rabaey, A. Chandrakasan and B. Nikolic. The additional textbooks 1 through 5 provide much additional information and can be quite useful.

Required Textbook: J. M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits*, Prentice Hall, 2003, ISBN:0130909963.

Additional Reading:

1. John P. Uyemura, *Introduction to VLSI Circuits and Systems: A Design Perspective* Prentice-Hall, Inc., 2002.
2. N. H. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Addison-Wesley, 2nd ed., 2004.
3. S.M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits Analysis & Design*, McGraw-Hill Inc., 2002.
4. H. Bhatnagar, *Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and PrimeTime*, 2nd edition, 2001
5. P. Kurup and T. Abbasi, *Logic Synthesis using Synopsys*, 2nd edition, 1997

Laboratory

Weekly design and simulation assignments using **Synopsys** CAD tools. Specifically, Synopsys tools will be used for logic synthesis, placement, routing and timing verification. HSPICE simulator will be used when necessary.

Weekly assignments will include synthesis, placement, routing and verification examples/tutorials using various tools. These tutorials will have existing HDL inputs and step-by-step instructions to learn the tools, which will lay the groundwork for a project implementation next quarter.

Tentative Schedule

Lectures and Labs:

Week	Lecture	Lab
1	Introduction to ASIC design	
2	FPGA and ASIC design	Logic Synthesis setup
3	No class (MLK day)	Logic Synthesis lab + 1 st Assignment
4	Introduction to Physical Design	Intro physical design lab
5	Floorplanning	Floorplanning lab
6	Placement	Placement lab, Midterm
7	No class (President's Day)	Midterm discussion
8	Routing	Routing lab
9	Multi-mode, Multi-corner Analysis	2 nd Assignment
10	Coping with Interconnect	

Academic Policies

The academic policies defined by the Office of Provost are upheld for this course. The complete list of policies (academic and otherwise) are listed at <http://www.drexel.edu/policies/>. The students should particularly be aware of the following policies:

Academic Integrity	http://www.drexel.edu/provost/policies/academic_dishonesty.asp http://www.drexel.edu/studentlife/judicial/honesty.html
Course Drop Statement	http://www.drexel.edu/provost/policies/course_drop.asp
Disability Statement	http://www.drexel.edu/oed/disabilityResources/
Student Conduct and Community Standards	http://www.drexel.edu/studentaffairs/community_standards/studentHandbook/

Course Change Policy: The instructor reserves the right to change the course during the quarter at his or her discretion. The changes, if applicable, will be communicated to the students verbally in class and reflected in the syllabus within the week of the change. Every effort will be made 1. Not to change any course policy past the course withdrawal period, 2. Collect student feedback prior to implementing any course change.